Temperature-Aware DVFS Scheduling for Deep-Drilling RISC-V Processors

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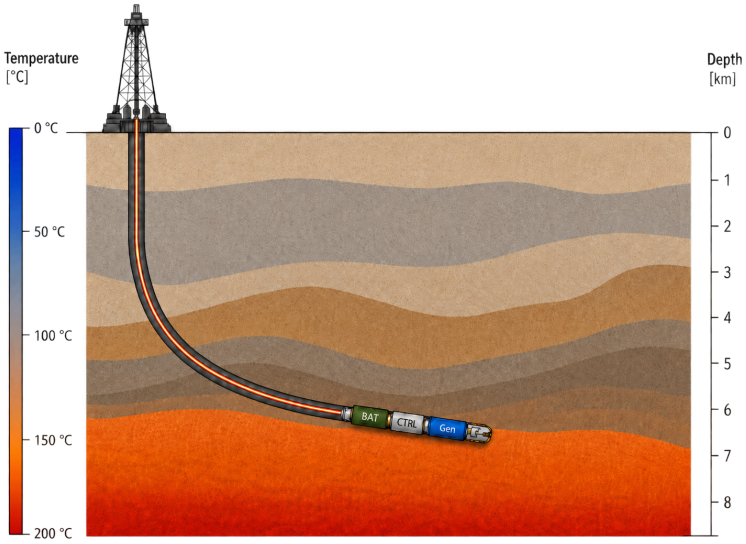
SRA, Leibniz University Hanover [(+)] IMS, Leibniz University Hanover
[(t)] Drilling Services, Baker Hughes, Celle

1. Deep-Drilling Constraints on Embedded Computing



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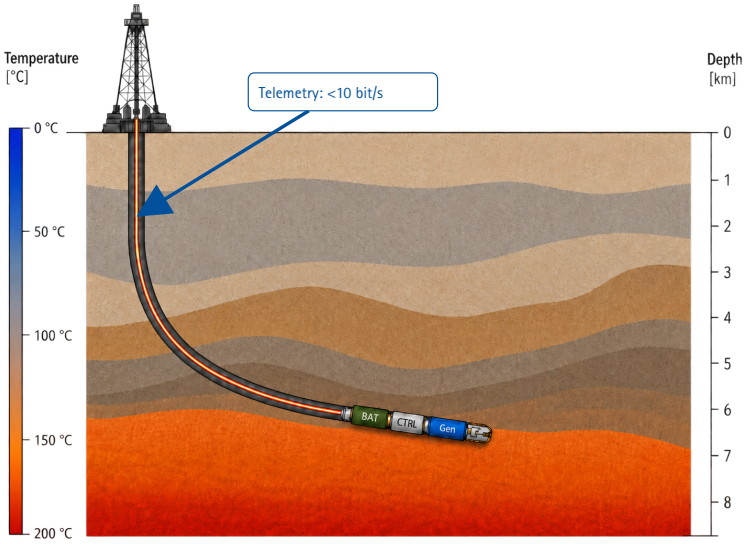

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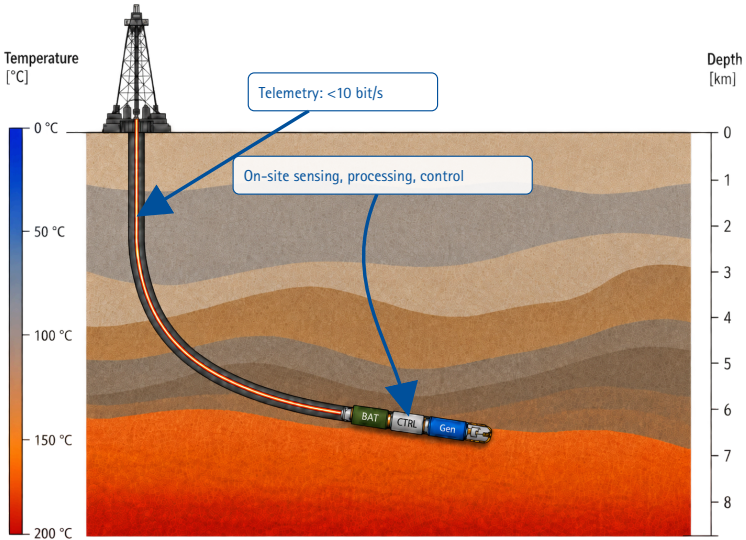

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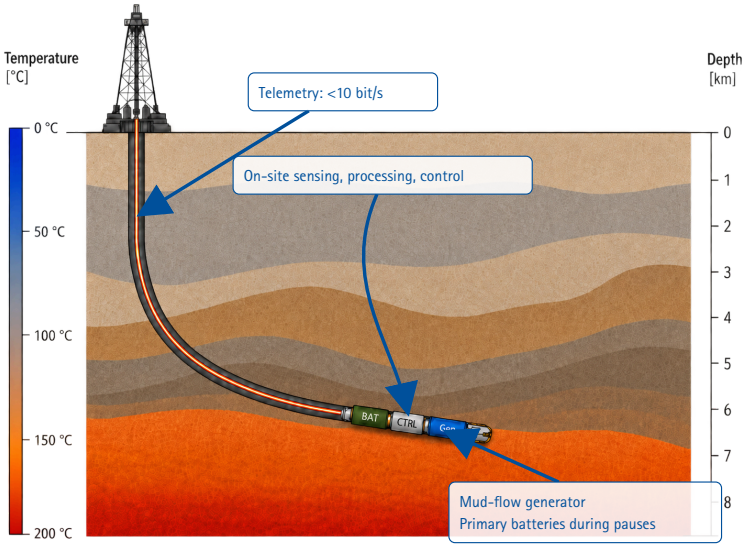

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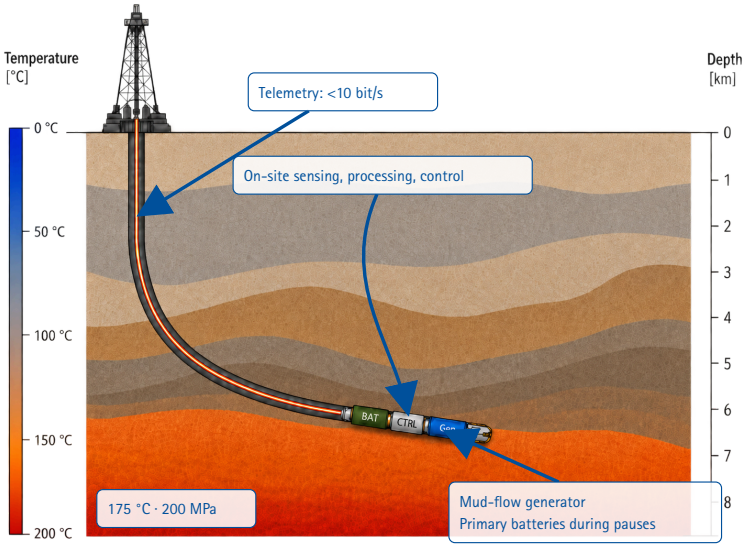

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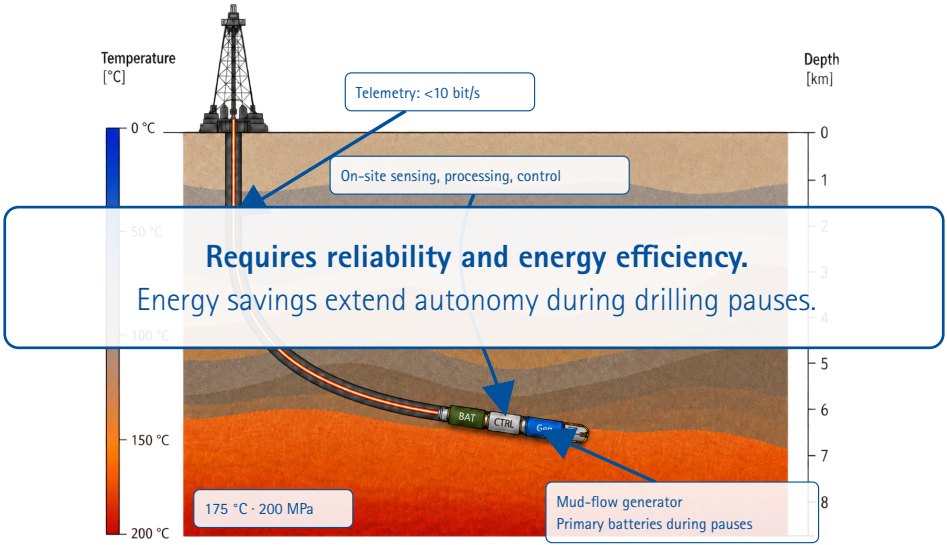
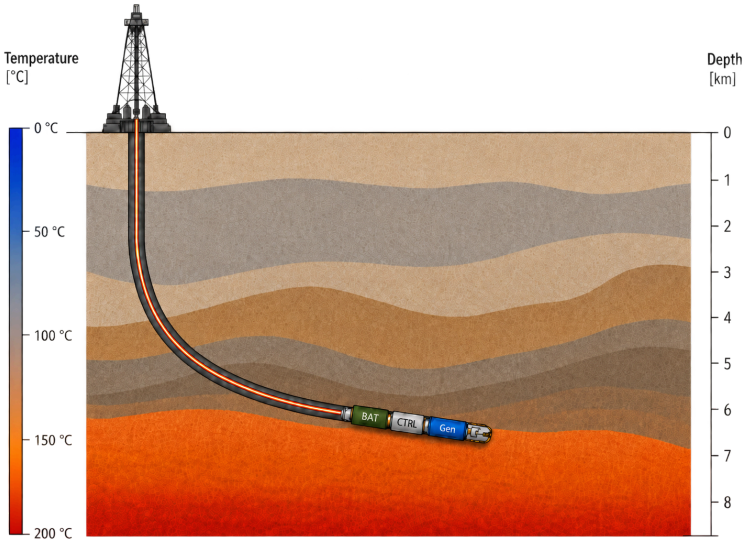


Requires reliability and energy efficiency.

Energy savings extend autonomy during drilling pauses.

2. Ambient-Dominated Thermal Conditions



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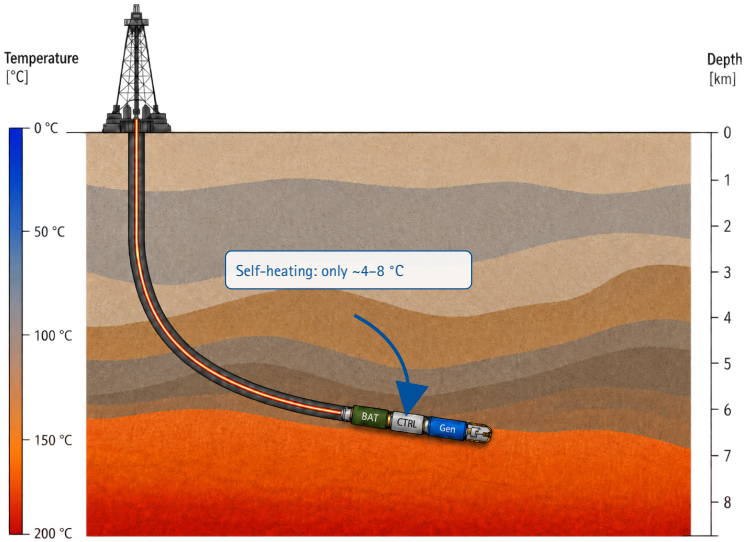

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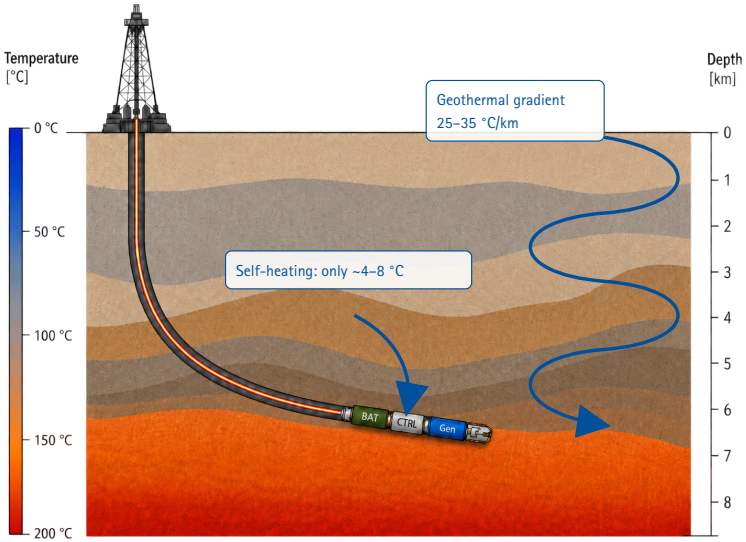

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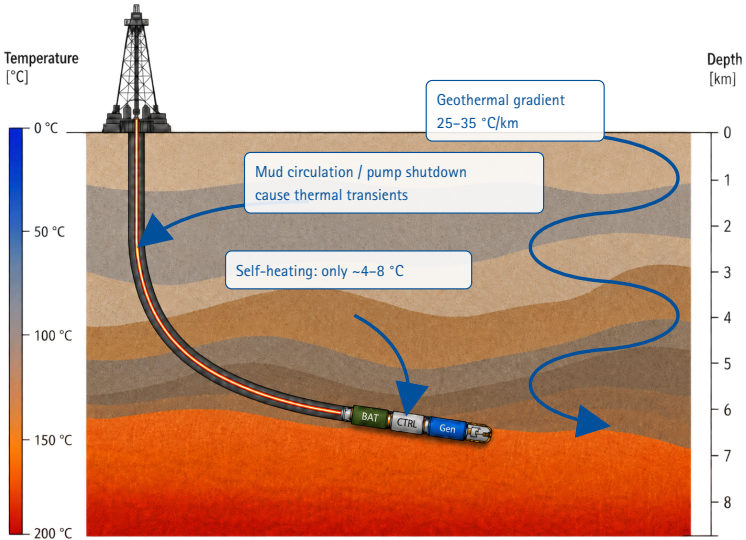

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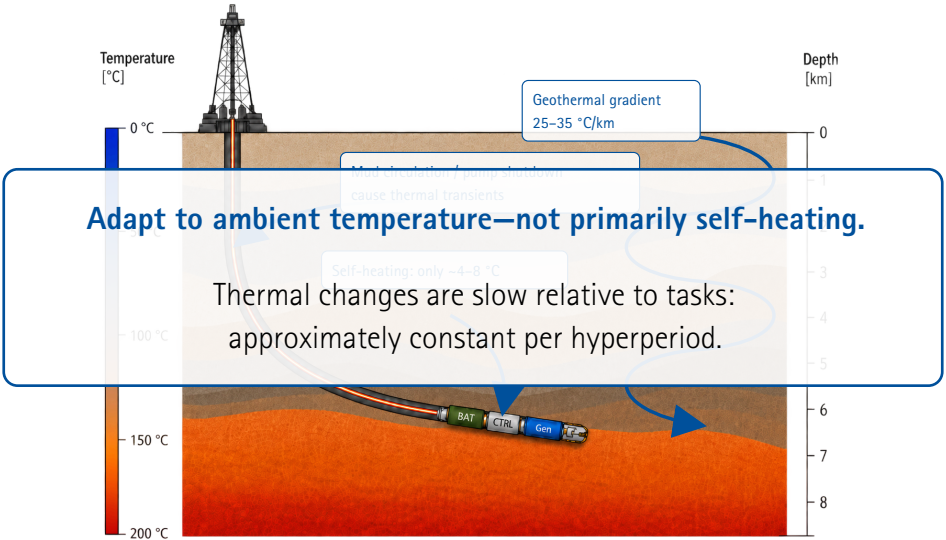


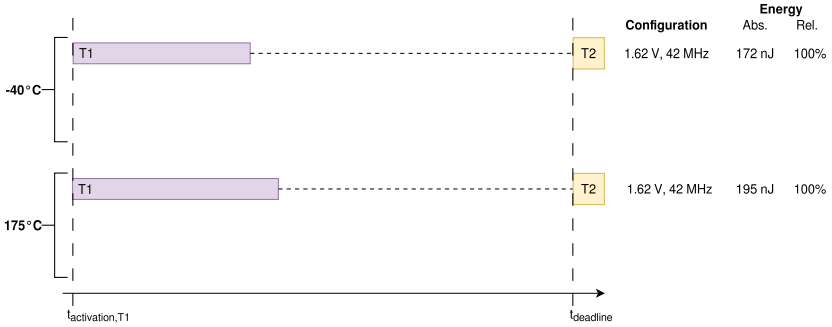
Adapt to ambient temperature—not primarily self-heating.

Thermal changes are slow relative to tasks:
approximately constant per hyperperiod.

3. Characteristics of High-Temperature SOI

X-FAB XT018: 180 nm silicon-on-insulator

- Static leakage below 1% of total power, even at 175 °C.
- Dynamic power dominates: $P_{\text{dyn}} \propto V^2 f$.



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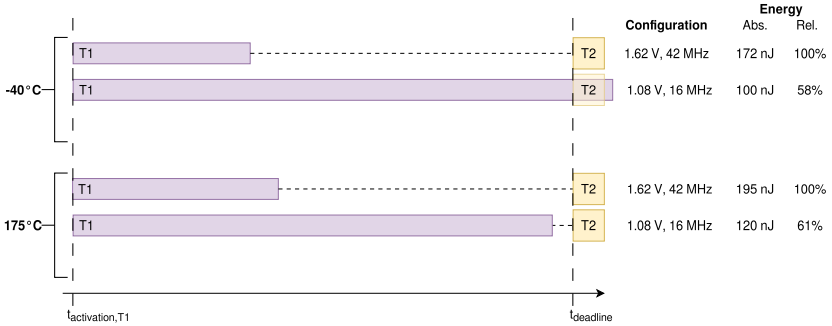

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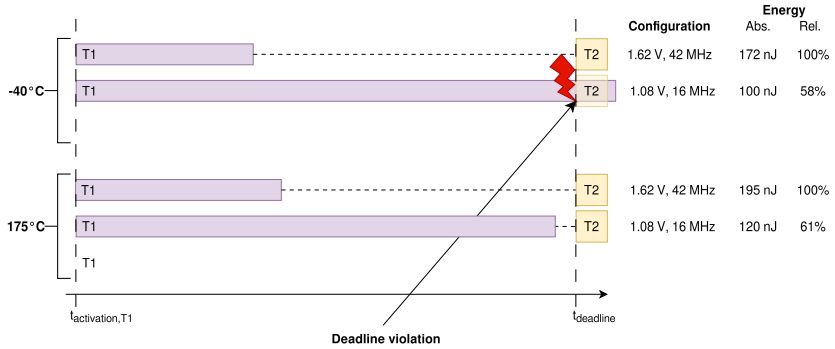

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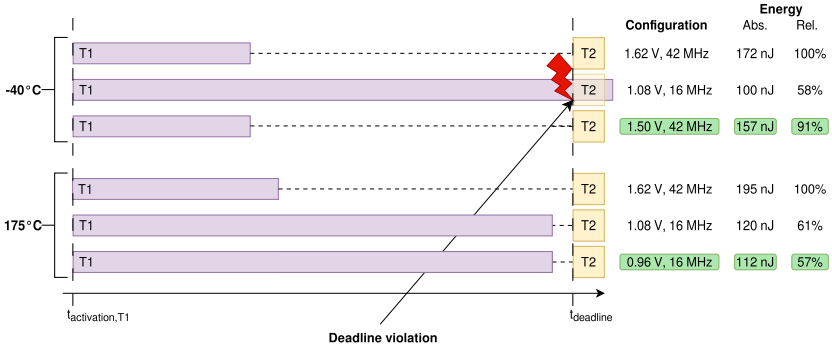

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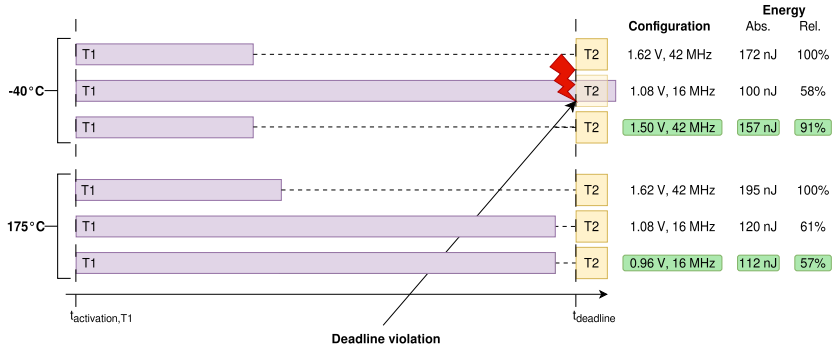
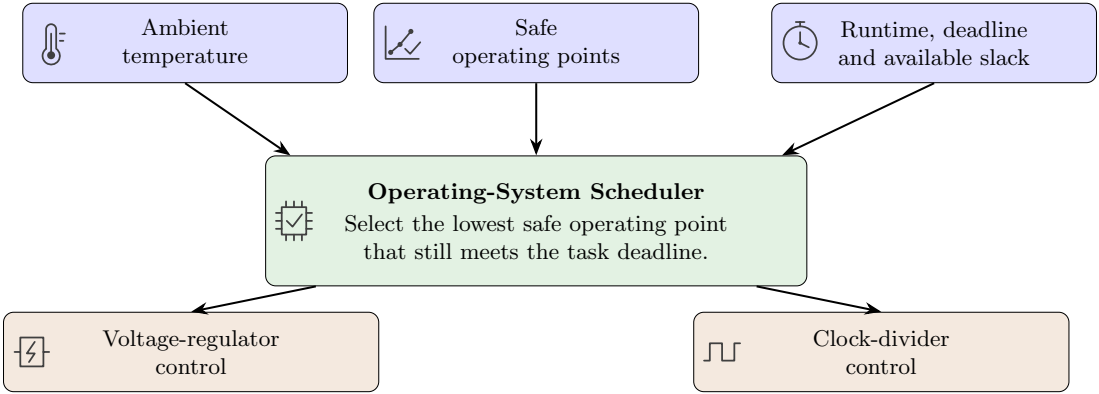


Timing-safe operating points depend on both voltage and temperature.

4. Hardware–OS Co-Design



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Timing limitation

Shortest observed runtime used in evaluation: **no formal deadline guarantee**.

In a real system use worst-observed execution times! (Analogue to worst-case execution time)

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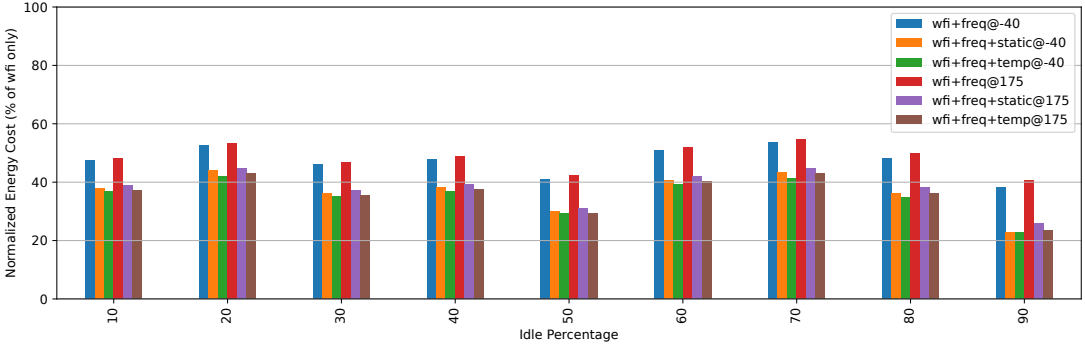

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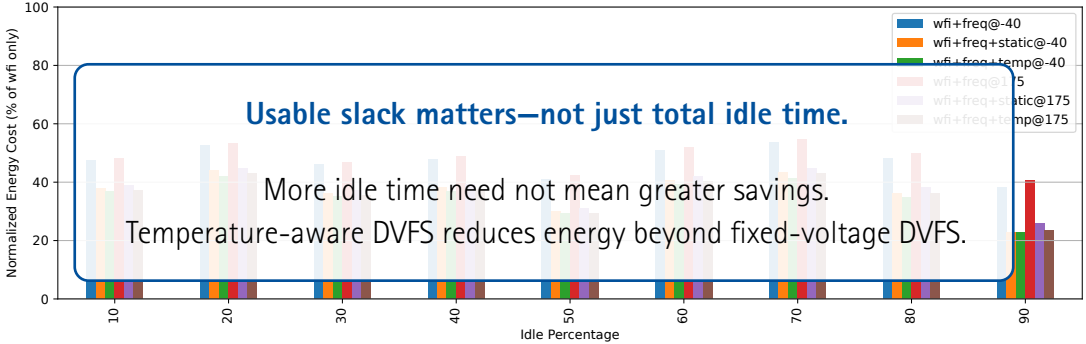

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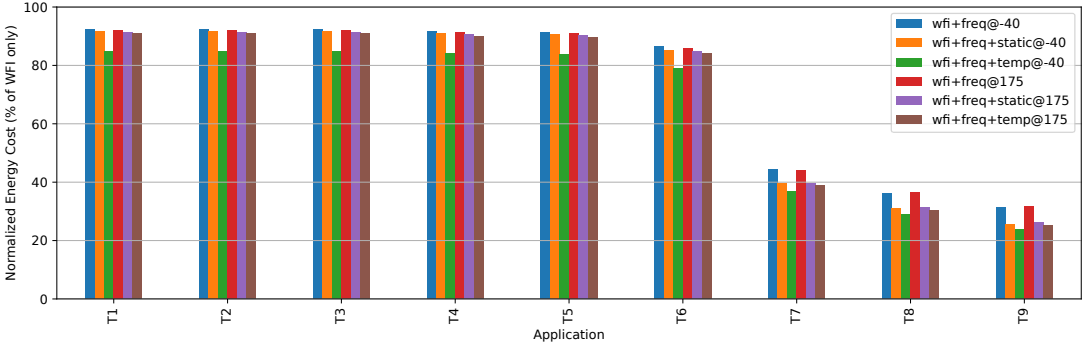

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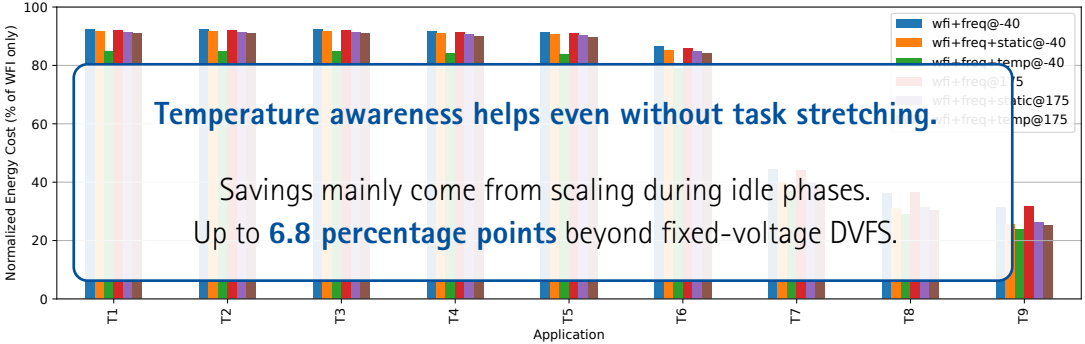

8. Conclusions and Limitations

- **Ambient temperature determines the thermal operating conditions.**
  - Temperature awareness is necessary for timing-safe DVFS.
- **Low-leakage SOI favors task stretching at reduced voltage.**
  - Slack becomes an opportunity for energy reduction.
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Next steps

Real measurements, manufacture the design

Apply findings to memory, peripherials, ...